The Influence of Ion-Implanted Profiles on the Performance of GaAs MESFET's and MMIC Amplifiers

DIMITRIS PAVLIDIS, SENIOR MEMBER, IEEE, JEAN-LOUIS CAZAUX, AND JACQUES GRAFFEUIL

Abstract—**The RF small-signal performance of GaAs MESFET's and MMIC amplifiers as a function of various ion-implanted profiles is theoretically and experimentally investigated. Implantation energy, dose, and recess depth influence are theoretically analyzed with the help of a specially developed device simulator. The performance of MMIC amplifiers processed with various energies, doses, recess depths, and bias conditions is discussed and compared to experimental characteristics. Some criteria are finally proposed for the choice of implantation conditions and process in order to optimize the characteristics of ion-implanted FET's and to realize process-tolerant MMIC amplifiers.**

I. Introduction

THE ELECTRICAL performance of GaAs MESFET's is greatly influenced by the doping profile of their active layer [1]–[3]. In addition, the rapid development of active layer fabrication techniques (VPE, MBE, ion implantation) allows the realization of almost any doping profile. Therefore, for discrete devices or monolithic integrated circuits, the doping has to be specially tailored to provide the best microwave performance.

In this paper, we analyze the influence of ion implantation conditions (dose, energy) and recess depth on the main elements of the MESFET equivalent circuit and on the microwave small-signal performance of ion-implanted MMIC amplifiers.

Section II describes the simulator used for our investigations and discusses some theoretical results obtained with it.

In Section III, the MMIC amplifier design is described together with the influence that dose, energy, and recess have on its performance. Finally, Section IV compares data to theoretical predictions for MESFET's and the MMIC amplifier.

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D. Pavlidis is with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122.

J.-L. Cazaux was with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor. He is now with Alcatel-Espace, Toulouse, France.

J. Graffeuil is with LAAS-CNRS and the University P. Sabatier, 07 Ave. Colonel Roche, 31400 Toulouse, France.

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II. The Simulator "SIMTEC"

A. Model Description

Several models for nonuniformly doped MESFET's have been reported [4]–[7]. The simulator described in this paper was developed in order to satisfy the following requirements: (i) to investigate any doping profile without the limitations imposed by equivalent profile transformations; (ii) to simulate submicrometer gate devices with short computation time (the influence of gate length on velocity is considered without performing long two-dimensional computations); and (iii) to compute all the elements of the equivalent circuit, including, for instance, the input gate resistance R_i, which is often neglected but strongly affects f_{max}.

The simulations presented below are based on a "hybrid" one-dimensional model involving an analytical formalism and numerical treatments of the classical equations of the "two-region" model [8]. In this way, it is possible to predict the performance of a GaAs MESFET with any doping profile described by a mathematical expression [7]. This model is, therefore, particularly suitable for ion-implanted MESFET's, where the doping profile shape depends on various parameters such as energy and dose of implantation.

A first description of this new simulator, called SIMTEC, has already been presented by the authors elsewhere [9]. From the MESFET geometrical dimensions and physical parameters given in Fig. 1 and Table I, the simulator SIMTEC yields for any doping profile and bias conditions V_{DS}, V_{GS} (Or I_{DS}):

- all the elements of the MESFET equivalent circuit except the series inductances (see Fig. 2 by way of example);
- the values of the current cutoff frequency f_T, the maximum oscillation frequency f_{max}, and the minimum noise figure F_{min}.

The model is suitable for submicrometer gate devices, the influence of velocity overshoot being taken into account by the following approximate relationship, proposed in

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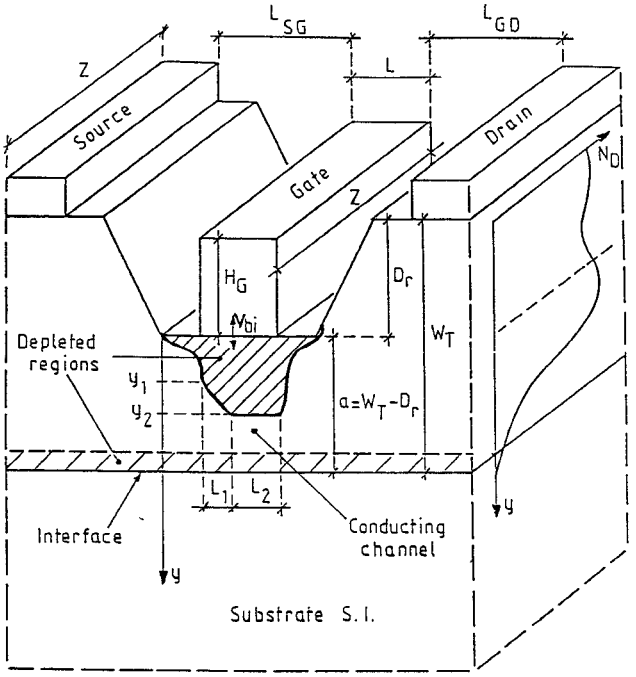


Fig. 1. Idealized cross section of MESFET devices used in this work.

TABLE I
GEOMETRICAL AND ELECTRICAL PARAMETERS USED IN THE MODEL (SIMTEC)

L	gate length
Z	total gate width
L_{SG}	source–gate spacing
L_{GD}	gate–drain spacing
D_r	recess depth
ρ_c	ohmic contact specific resistance
V_{bi}	Schottky barrier built-in potential
H_G	gate metallization height
N_k	number of gate fingers of width z ($Z = N_k \cdot z$)
ρ_G	gate metal resistivity
R_{TH}	thermal resistance

The values of L_{SG}, L_{GD}, D_r, ρ_c, H_G, ρ_G, and N_k make it possible to determine the access resistances R_S, R_D, and R_G.

[10]:

$$v_{\text{sat}} = 60L^{-0.56} \tag{1}$$

where L is the gate length (m) and v_{sat} the equivalent saturated velocity (m/s). This relationship gives a realistic effective saturation velocity v_{sat}, which is larger than the steady-state velocity. Thus v_{sat} is 1.4×10^5 m/s if $L=1$ μm and reaches the effective value of 2.7×10^5 m/s if $L=0.3$ μm.

For reduced computation times, the mobility is assumed to have a constant average value μ_0 across the active layer. SIMTEC can, however, accept precise functions $\mu_0(y)$ for the mobility profile. The influence of ionized impurities on the average mobility is approximated by

$$\mu_0(\text{cm}^2\text{V}^{-1}\text{s}^{-1}) = \frac{8000}{1+\left[\dfrac{Neq}{10^{17}}\right]^{1/2}} \tag{2a}$$

where Neq (cm^{-3}) is the average impurity concentration,

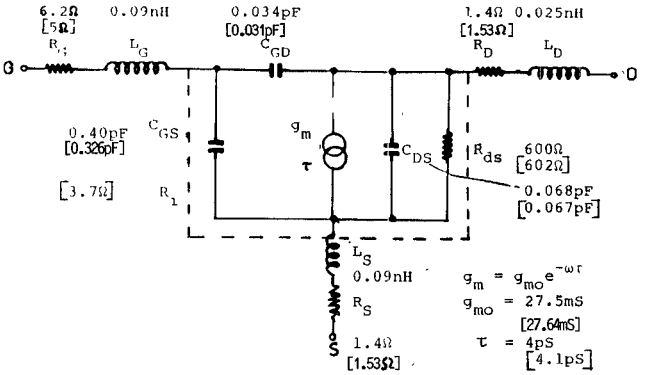


Fig. 2. FET equivalent circuit de-embedded from S-parameter measurements and predicted by theory (in brackets). Implantation conditions: $E_1 = 60$ keV, $D_1 = 20\times10^{12}$ cm^{-2}, and $E_2 = 250$ keV, $D_2 = 6\times10^{12}$ cm^{-2}. Bias point: $V_{DS} = 3$ V, $I_{DS} = 30$ mA. A recess depth of 0.14 μm provides $V_T = -3.6$V.

given by

$$Neq = \frac{\left[\int_0^\infty N_D(y)\,dy\right]^2}{2\int_0^\infty N_D(y)\,y\,dy} \tag{2b}$$

$N_D(y)$ being the doping density. Therefore the mobility degradation for the highest doping densities [11] is systematically considered in our simulations.

Two-piece velocity–electric field characteristics are employed using the following relations:

$$v(E) = \frac{\mu_0 E}{1+E/E_0} \qquad \text{if } E \leqslant E_s \tag{2c}$$

and

$$v(E) = v_{\text{sat}} \qquad \text{if } E > E_s \tag{2d}$$

where E_0 is a parameter with electric field dimensions equal to 2.5×10^6 Vm^{-1}. E_s is the saturation electric field ($E_s = v_{\text{sat}}/(\mu_0 - v_{\text{sat}}/E_0)$).

The simulator has two additional features. The first is that the Debye transition zone between the depletion layer and the conducting channel can be taken into account in the computations. The model can indeed distinguish optionally between free electron and shallow level impurity concentrations. By solving the semiconductor equations at all points of the channel, one can remove the limitation of abrupt transition between the depleted and neutral part of the channel. This results in a precise calculation of the free carrier distribution $n(y)$, which over several Debye lengths $\lambda_D = [\epsilon KT/q^2 N_D(y)]^{1/2}$ is equal to neither zero nor $N_D(y)$.

The second additional feature is that the presence in the semi-insulating substrate of deep levels (EL_2, for example) forming an N–I junction with the N-doped layer of the MESFET [12] can also be accounted for.

These optional capabilities were not retained in this work in order to simplify the analysis and minimize computation time. At given bias conditions, the execution time could therefore be less than 0.1 s for dc and small-signal simulation on an IBM 3080 computer. This is many orders

of magnitude less than a numerical simulation [13]. Therefore, SIMTEC is very suitable for the computer-aided design of low-complexity circuits.

B. Method of Element Calculation

The basic device structure used in the simulations is shown in Fig. 1. The technology parameters of Table II were maintained constant throughout this work and correspond to the fabricated devices. For every implantation condition (energy, dose) or recess depth, all the elements of the model (Fig. 2) are calculated, with the exception of L_S, L_D, and L_G. The computation is based on the solution of the following system of equations.

1) Linear (Ohmic) Operation Equations: These are derived from Poisson's equations by considering the current I_{DS} across the channel and the drain–source V_{DS} and gate–source V_{GS} voltages:

$$V_{bi} + R_S I_{DS} - V_{GS} = \frac{q}{\epsilon}\int_0^{y_1} y N_D(y)\,dy \tag{3}$$

$$V_{DS} - (R_S + R_D) I_{DS} = \frac{q}{\epsilon}\int_{y_1}^{y_2} y N_D(y)\,dy \tag{4}$$

$$I_{DS}\left(L + \frac{q}{\epsilon E_0}\int_{y_1}^{y_2} y N_D(y)\,dy\right) = \frac{q^2 Z}{\epsilon}\int_{y_1}^{y_2}\left(\int_y^a \mu_0(y') N_D(y')\,dy'\right) y N_D(y)\,dy. \tag{5}$$

2) Saturation Operation Equations: The two-region model [8] is employed. Equations (3) and (5) can be used again in linear region I by replacing L with L_1. In region II carrier propagation is at the saturated velocity v_{sat} and the following equation holds:

$$I_{DS} = q v_{sat} Z \int_{y_2}^{a} N_D(y)\,dy. \tag{6}$$

Using the method of Grebene and Ghandi [14] for the solution of the two-dimensional Poisson's equation and defining an equivalent channel thickness a_s as

$$a_s = \frac{I_{DS}}{q v_{sat} Z N_D(y_2)} + y_2 \tag{7}$$

we obtain

$$V_{DS} - (R_S + R_D) I_{DS} = \frac{q}{\epsilon}\int_{y_1}^{y_2} y N_D(y)\,dy + \frac{2 a_s E_s}{\pi}\sinh\left(\frac{\pi(L - L_1)}{2 a_s}\right). \tag{8}$$

Depending on the operating conditions V_{DS}, V_{GS}, the static parameters of the MESFET can be obtained by numerical solution of either (3)–(5) (evaluation of y_1, y_2, I_{DS} in linear mode) or (3), (5)–(8) (evaluation of a_s, y_1, y_2, L_1, I_{DS} in saturation mode). The equivalent circuit parameters g_{m0}, R_{DS} are obtained from the ratio of the incremental change of drain current ΔI_{DS} to the incremental change of intrinsic drain ΔV_{DS} and gate voltage ΔV_{GS}. C_{GS} is evaluated using the transmission line approach described in the Appendix. These calculations can be performed with the help of the static equations given above. For the exact calculation of R_{DS}, we included the effects of carrier injection into the semi-insulating substrate by considering a parallel connected parasitic resistance R_{DS_p}. This resistance is found to be proportional to the length $L - L_1$ of the saturated region [9].

TABLE II
CONSTANT PARAMETERS USED IN THE SIMULATION IRRESPECTIVE OF DOPING PROFILE

L	1 μm
Z	300 μm
L_{SG}	1.75 μm
L_{GD}	1.75 μm
V_{bi}	0.75 V

The significance of L, Z, L_{SG}, and L_{GD} is given in Fig. 1. V_{bi} is the built-in gate voltage.

The access inductances L_S, L_D, L_G are not calculated with the program and were extracted from experimental S-parameter data.

The source and drain series resistances R_S and R_D consist of a contact resistance R_{SC} in series with the lateral active layer resistance R_{SL}. R_{SC} is a function of the specific contact resistivity ρ_c, which in turn depends on the doping value N_D in the region below the ohmic contact. A two-region expression is used for the evaluation of ρ_c [15]:

$$\rho_c = \frac{10^{15}}{\mu_0 N_D} \qquad \text{for } N_D \leq 4.7\times 10^{17}\ \text{atoms}\cdot\text{cm}^{-3} \tag{9a}$$

$$\rho_c = \frac{10^{15}}{\mu_0 4.7\times 10^{17}} \qquad \text{for } N_D > 4.7\times 10^{17}\ \text{atoms}\cdot\text{cm}^{-3}. \tag{9b}$$

The active layer resistance can be computed from the following expression.

$$R_{SL} = \int_0^{L_{SG}} \frac{dx}{Zq\int_0^{W(x)} N_D(y)\mu(y)\,dy}. \tag{10}$$

$W(x)$ is the active layer thickness and varies with x because of gate recess.

The evaluation of the intrinsic channel resistance R_i is based on a method described in the Appendix. The drain–source (C_{DS}) and gate–drain (C_{GD}) capacitances are finally calculated from the coupling between metal strips [16], [17]. The results of Fig. 2 show the excellent agreement between theoretical and experimental equivalent circuit data for an ion-implanted FET. The fringing capacitance (C_{GSf}) between source and gate metallizations is included in the calculation of C_{GS}. The experimental values were obtained by fitting calculated to measured S-parameter data in the frequency range of 2 to 18 GHz.

C. Implantation Dose Influence on MESFET Performance

The simulated transistors had active layers realized by a two-step Si^{29} ion implantation through a 500 Å thick Si_3N_4 cap. The first implantation was done at an energy $E_1 = 60$ keV and dose $D_1 = 20\times10^{12}$ cm^{-2}. These conditions were maintained the same throughout our investigations and resulted in a high doped N^+ surface layer. The second implantation had variable energies and doses. To examine the influence of dose, the energy was fixed at $E_2 = 250$ keV and the dose was varied from $D_2 = 3\times10^{12}$ cm^{-2} to 20×10^{12} cm^{-2}. For every D_2 value, the recess depth (D_r) is adjusted to yield a constant threshold voltage $V_T = -3.6$ V (from $D_r = 770$ Å for $D_2 = 3.10^{12}$ cm^{-2} to $D_r = 2220$ Å for $D_2 = 20\times10^{12}$ cm^{-2}).

The most relevant results are given in Fig. 3(a)–(c) and were obtained for constant $V_{DS} = 3$ V, $I_{DS} = 30$ mA bias. The intrinsic transconductance g_{m0} and gate capacitance C_{GS} are found to increase monotonically with dose (Fig. 3(a)). This is understood by noting that the recess depth was increased with the dose in order to maintain a constant threshold voltage. The thickness of the active layer below the gate was therefore thinner for high doses and resulted in higher g_{m0} and C_{GS}, as expected from the approximated expressions [18]

$$g_{m0} = \frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{\epsilon Z v_{\text{sat}}}{y_d} \tag{11a}$$

$$C_{GS} = \frac{\Delta Q}{\Delta V_{GS}} = \frac{\epsilon ZL}{y_d} \tag{11b}$$

where the depletion region thickness y_d is given by

$$y_d = \left[\frac{2\epsilon}{qN_D}(V_{bi} - V_{GS})\right]^{1/2}. \tag{11c}$$

Since the average donor concentration increases with dose, R_{DS} decreases with D_2, as shown in Fig. 3(b). R_i is also found to increase with dose. The parameters responsible for the latter change are, first, the higher doping N_D and, second, the smaller channel thickness $a - y(x)$. The nonuniform $R_i(x)C_{GS}(x)$ transmission line under the gate has a resistance $R_i(x)$ per unit length which is inversely proportional to the $N_D(a - y(x))$ product. The rate at which N_D increases is obviously smaller than the corresponding thickness variations $a - y(x)$ necessary to maintain a constant threshold. This results in an overall increase of R_i with dose.

The current cutoff frequency $f_T = g_{m0}/2\pi C_{GS}$ remains almost constant with dose (Fig. 3(c)) since the g_{m0} and C_{GS} variations are very similar (see Fig. 3(a)). However, the largest $f_{\max}$ values (Fig. 3(c)) are obtained for small doses because R_i is, in this case, very small (see Fig. 3(b) and [18]], [19]). The strong dependence of $f_{\max}$ on R_i demonstrates the need for very precise R_i evaluations to permit good understanding of the device microwave performance.

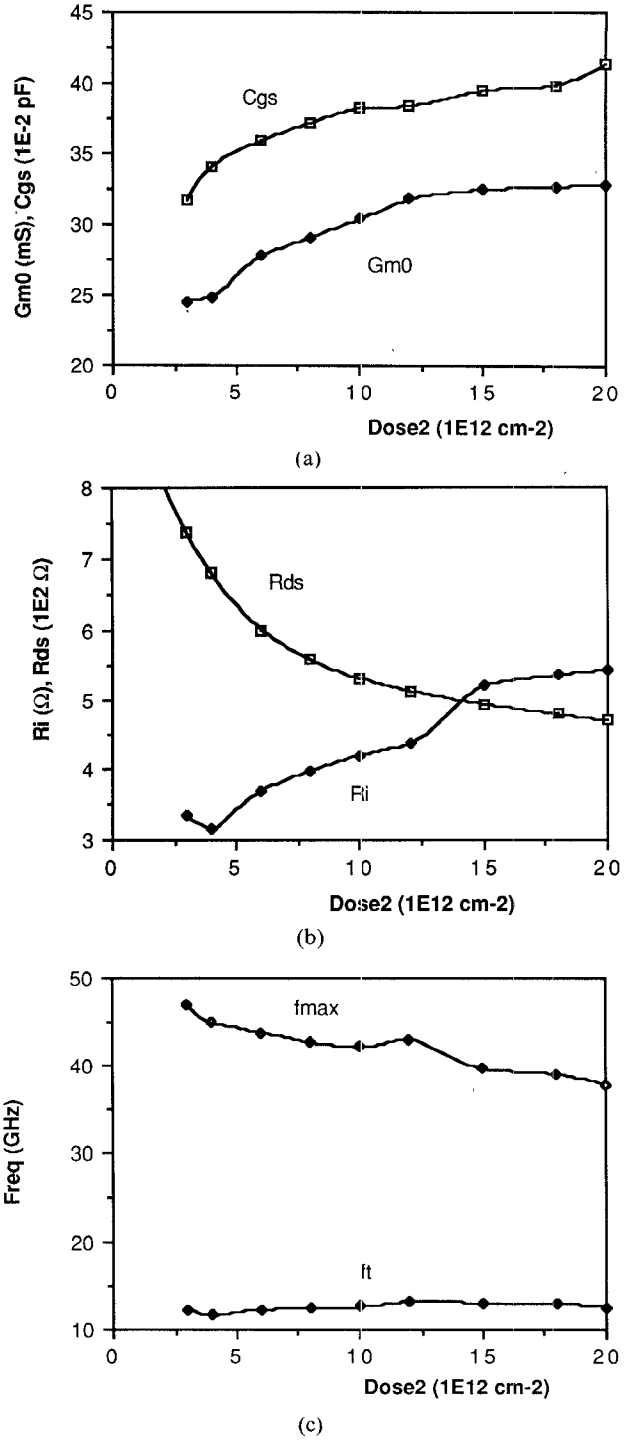
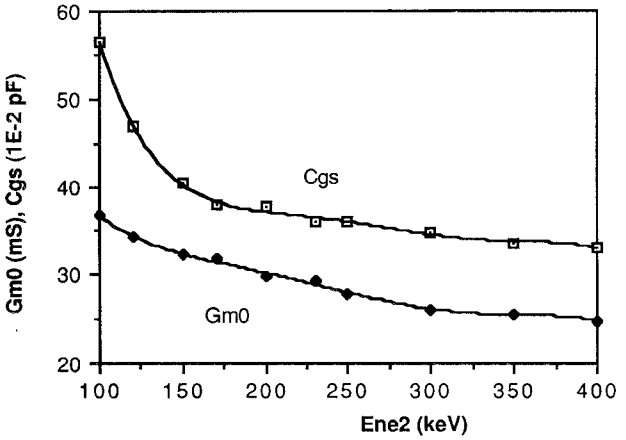


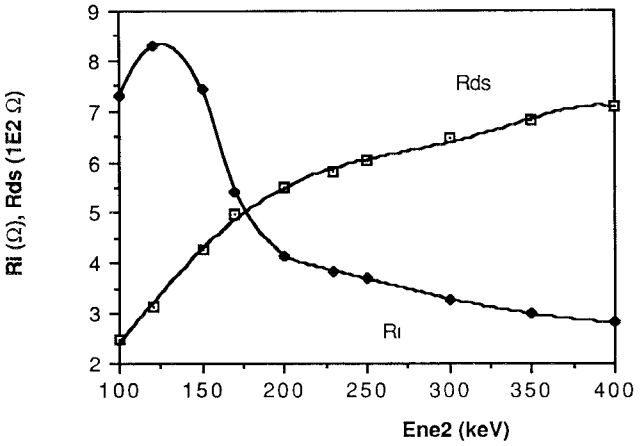
Fig. 3. Influence of implanted dose on: (a) C_{GS}, g_{m0}, (b) R_{DS}, R_i, and (c) f_T and $f_{\max}$ for an FET (300 μm$\times$1 μm, $V_{DS} = 30$ mA) implanted with $E_2 = 250$ keV. D_2 varies between $= 3\times10^{12}$ cm^{-2} and 20×10^{12} cm^{-2}, and gate recess was kept constant for $V_T = -3.6$V.

D. Implantation Energy Influence on MESFET Performance

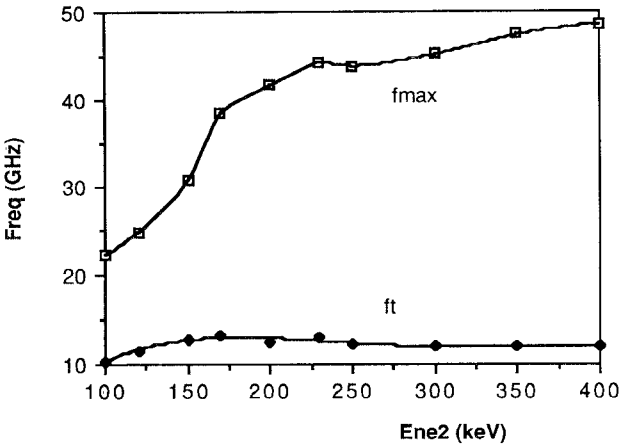
To investigate the influence of implantation energy, the dose of the second implants was kept constant at $D_2 = 6\times10^{12}$ cm^{-2}, and the energy varied from 100 keV to 400 keV. The recess depth was adjusted up to 2930 Å for $E_2 = 400$ keV in order to yield a constant threshold voltage $V_T = -3.6$ V. The bias conditions were $V_{DS} = 3$ V, $I_{DS} = 30$ mA.



(a)



(b)



(c)

Fig. 4. Influence of implantation energy on (a) C_{GS}, g_{m0}, (b) R_{DS}, R_i, and (c) f_T and $f_{\max}$ for an FET (300 μm$\times$1 μm, $V_{DS}=30$ mA) with constant implanted dose $D_2=6\times10^{12}$ cm^{-2} and energy E_2 varying between 100 keV and 400 keV. V_T was kept constant, equal to -3.6 V.

The active layer thickness increases with implantation energy. At higher energies and for recessed devices with the same V_T, the average donor concentration is lower in the channel below the gate. The associated depletion thickness is therefore larger. The g_{m0} and C_{GS} changes with implantation energy (Fig. 4(a)) can thus be explained by depleted region extension. These results are in good agreement with the previously reported work of Trew [2].

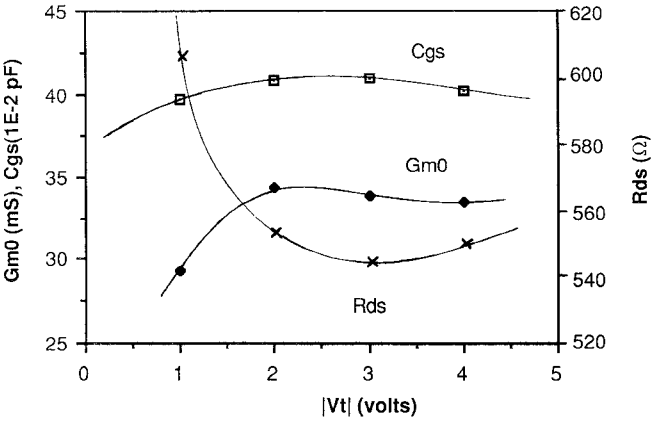


Fig. 5. Influence of threshold voltage (V_T) on C_{GS}, g_{m0}, R_{DS} for an FET (300 μm$\times$1 μm, $V_{DS}=3$ V, $I_{DS}=I_{DSS}/2$), implanted with $E_2=250$ keV, $D_2=6\times10^{12}$ cm^{-2}. Different recess depths to obtain different V_T values.

The lower average donor concentrations are also responsible for the increase of R_{DS} with implantation energy (Fig. 4(b)). R_i decreases with E_2 at values above 120 keV; at high energies, the low N_D's have to be compensated by larger channel thicknesses to maintain $V_T=$ constant, resulting therefore in smaller R_i's.

It can again be noted that f_T is not very sensitive to energy variations of implantation (Fig. 4(c)). However, $f_{\max}$ is increased with energy due to both the reduction of the input resistance R_i and the increase of R_{DS}.

E. Gate Recess Depth Influence on MESFET Performance

For these investigations, the dose and energy of the second implants were maintained constant to $D_2=6\times10^{12}$ cm^{-2} and $E_2=250$ keV. The bias conditions were $V_{DS}=3$ V and $I_{DS}=I_{DSS}/2$, where I_{DSS} is the drain–source saturation current at $V_{GS}=0$ V. (For instance, $I_{DS}=45$ mA when $V_T=-3.6$ V.) The choice of these conditions allows device comparison since the absolute I_{DSS} value varies with recess. The recess depth was varied to obtain threshold voltages V_T between 1 and 5 V.

The variations of g_{m0}, C_{GS}, and R_{DS} with recess are shown in Fig. 5. The high g_{m0} values at small recess depths (high V_T's) are explained by the higher average carrier concentration when the complete implantation profile is available. When the recess depth is high, then the carrier distribution under the gate corresponds primarily to the tail of the profile and is therefore low, with the result of a small transconductance [18].

The slight increase of C_{GS} with V_T is again due to the higher carrier concentration $n(y)$ at small recess depths. This is equivalent to smaller depletion thicknesses and consequently higher capacitance at large dopings.

R_{DS} increases with recess depth (small V_T) since the channel doping density is, in this case, relatively small. Similar behavior is also observed for R_i.

The frequencies f_T and $f_{\max}$ are increasing with V_T due to the faster changes for g_{m0} than C_{GS}.

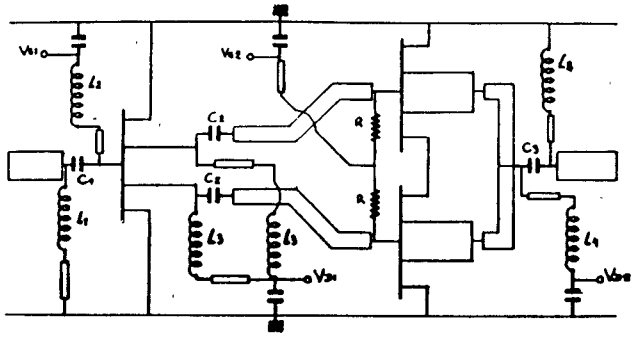


Fig. 6. Circuit diagram of the two-stage amplifier optimized by the SIMTEC FET model.

III. Amplifier Design Using the Developed Model

The FET model presented above has been successfully used in the design of microwave monolithic integrated GaAs amplifiers. It provides information regarding the influence that bias voltages, as well as implantation dose (D), energy (E), and threshold voltage (V_T), have on the amplifier electrical characteristics. Small-signal gain (G) and input and output SWR (SWR_{in} and SWR_{out}) can thus be examined with respect to their sensitivity to material parameters (D, E) and operating conditions. Circuit sensitivity to processing such as recess depth can also be considered by V_T simulations. The understanding of the above phenomena is of primary importance in the optimization of monolithic amplifiers since it makes it possible to design IC's which are tolerant to technology variations.

A. Amplifier Structure

Fig. 6 shows the circuit diagram of a two-stage monolithic amplifier designed with the tree approach [20], [21] and optimized with the model described in the previous sections. Each FET cell has a 1 μm gate length and a width of 600 μm, the total output periphery being consequently 1200 μm. Instead of using hybrid divider networks to feed the gates of a single transistor with large periphery, the tree approach uses the intrinsic isolation characteristics of FET's to divide the signals which have been amplified by the previous stages. It also uses several individual cells instead of a single large-periphery FET. The output combining network is made in lumped form and provides signal matching and dc biasing. These features allow the realization of compact power amplifier designs with no phasing or matching problems since individual cells have modest gate widths and do not suffer from impedance lowering. The amplifier of Fig. 6 was optimized for maximum small-signal gain and minimum input and output SWR over the frequency range of 6.0 to 7.0 GHz. It was intended for 10 percent bandwidth operation around the center frequency $f = 6.5$ GHz. The gain roll-off over the operating bandwidth is 1.7 dB and reflects the best compromise for maximum gain and matched input–output. Large-signal characterization is outside the scope of this paper and can be studied by other models [22]; these take into consideration the change of the FET output resistance

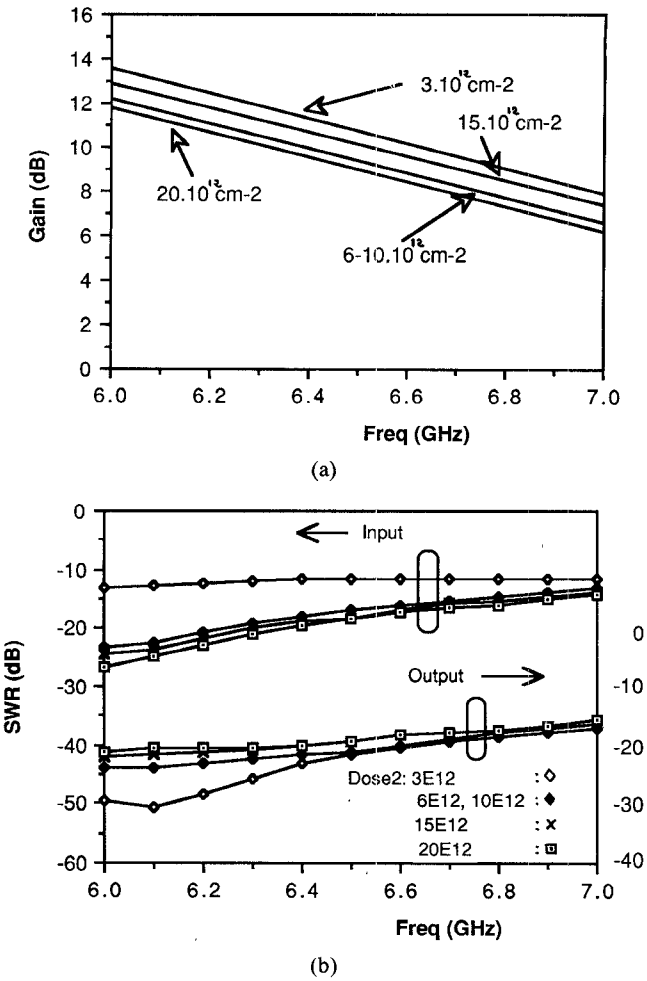


Fig. 7. Optimized amplifier performance and influence of implantation dose on (a) gain and (b) input and output SWR.

R_{DS} with driving power and modify accordingly the previously optimized small-signal characteristics. The small-signal model used for the amplifier design is given in Fig. 2.

B. Dose Influence on Amplifier Performance

The optimized amplifier characteristics are shown in Fig. 7(a) and (b) together with the influence that dose variations have on the gain and SWR. In both cases, (a) and (b), the transistors have the same implantation energy ($E_2 = 250$ keV) and threshold voltage ($V_T = -3.6$ V), so that the influence of dose D_2 can be studied alone. By decreasing the dose, the output resistance R_{DS} increases (Fig. 3(b)), and the input capacitance C_{GS} and transconductance g_m decrease (Fig. 3(a)) as outlined in the previous section. The changes in the values of the FET parameters with implanted dose can therefore be understood by considering the maximum unilateral gain of the FET, which is approximated by the following formula:

$$GMU \approx \frac{1}{16\pi^2}\frac{1}{f^2}\left(\frac{g_m}{C_{GS}}\right)^2 \frac{R_{DS}}{R_i + R_g + R_s} \qquad (12)$$

where R_i and R_g are the intrinsic and metal resistance of the gate (see Fig. 2), and f is the frequency of operation. When the dose decreases from 6×10^{12} cm^{-2} to 3×10^{12}

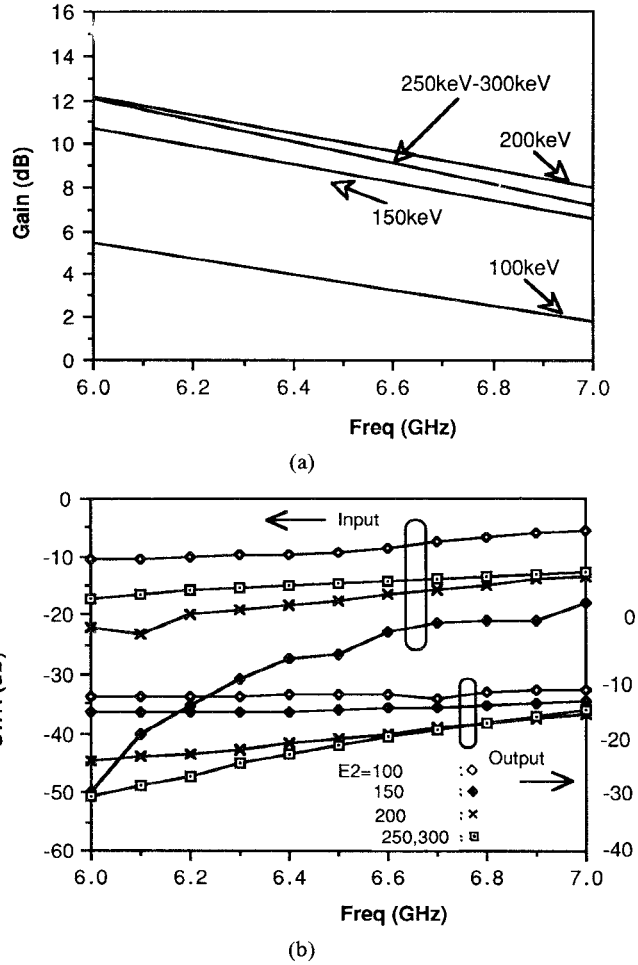


Fig. 8. Amplifier characteristics as a function of implantation energy. (a) Gain. (b) Input and output *SWR*.

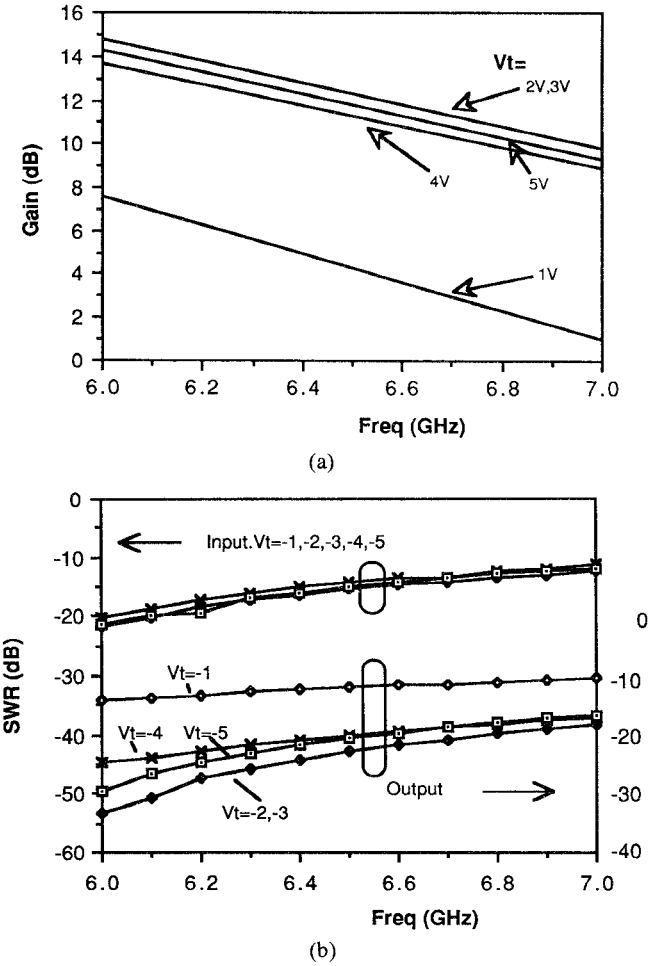


Fig. 9. Influence of threshold voltage V_T (recess) on the amplifier performance for a FET implanted with $E_2 = 250$ keV, $D_2 = 6\times10^{12}$ cm^{-2}. (a) Gain. (b) Input and output *SWR*.

cm^{-2}, R_{DS} changes faster than the g_m/C_{GS} ratio, resulting in FET's with improved *GMU*. This results in turn in higher amplifier gain with slightly improved output matching characteristics. The gate capacitance decrease is, however, so large that the input *SWR* of the amplifier is degraded. Although C_{GS} decreases rapidly for doses smaller than 6×10^{12} cm^{-2}, it shows relatively invariant characteristics for D_2's up to 20×10^{12} cm^{-2}. This explains the large amplifier mismatch at 3×10^{12} cm^{-2} compared to 20×10^{12} cm^{-2}. The results suggest that the influence of implanted dose on circuit performance is very small.

C. Energy Influence on Amplifier Performance

Implantation energy variations seem to have a more pronounced influence on circuit performance. The results of Fig. 8(a) and (b) show G, SWR_{in}, and SWR_{out} curves of the two-stage amplifier for E_2 energy variations between 100 and 300 keV (in all cases $D_2 = 6\times10^{12}$ cm^{-2}). Gate recess was again adjusted so that all FET's show the same $V_T = -3.6$ V value. As the energy E_2 decreases from 300 keV to 250 keV, the transconductance g_m and gate capacitance increase (Fig. 4(a)), but the output resistance R_{DS} decreases (Fig. 4(b)). These changes compensate each other and no substantial FET or amplifier performance variation is therefore observed between the nominal energy of 250 keV and $E_2 = 300$ keV. For energies between 250 keV and 200 keV, the R_{DS} variation becomes slightly stronger than the g_m/C_{GS} change and the unilateral gain improvement of the FET produces a slight increase of amplifier gain at $E_2 = 200$ keV. By further decreasing the energy, the output mismatch of the amplifier, caused by the rapid R_{DS} variations, results in steadily smaller gains and higher SWR_{out}. As far as the amplifier input is concerned, the slight increase of C_{GS} when decreasing the implanted energy from 300 keV to 150 keV seems to favor impedance matching. This is due to the input matching network being not perfectly optimized for the nominal energy $E_2 = 250$ keV, since a compromise had to be made in optimizing simultaneously G, SWR_{in}, and SWR_{out}. For even smaller energies, ($E_2 = 100$ keV), C_{GS} is dramatically increased and causes pronounced amplifier mismatch.

D. Recess Depth Influence on Amplifier Performance

The influence of recess on the amplifier performance is shown in Fig. 9(a) and (b). The nominal energy ($E_2 = 250$ keV) and dose ($D_2 = 6\times10^{12}$ cm^{-2}) are used here for a FET with different threshold voltages V_T. The g_m and C_{GS} parameters increase initially with threshold voltages ($V_T =$

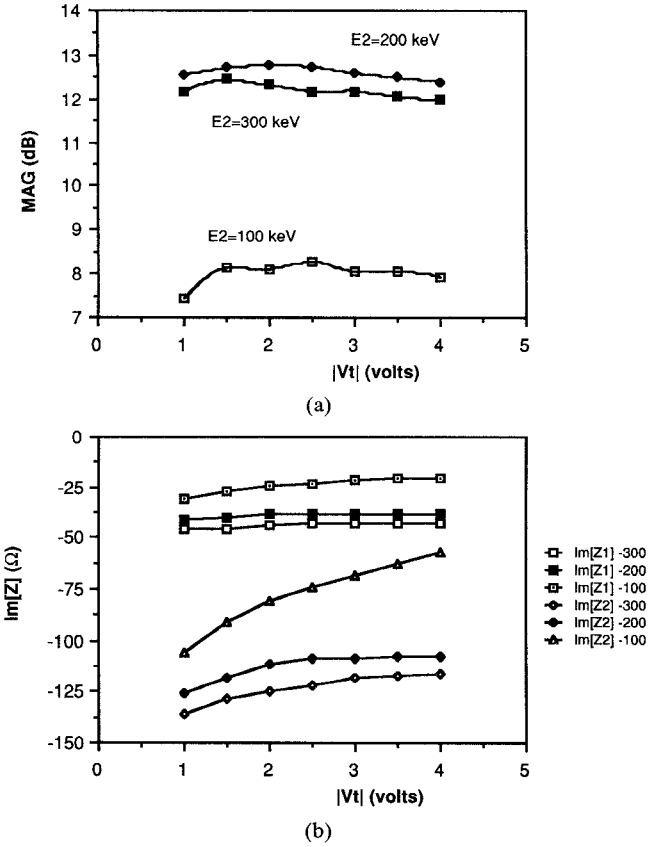


Fig. 10. (a) Maximum available gain (*MAG*) of MESFET (300 μm×1 μm) at $f = 6.5$ GHz as a function of recess (threshold voltage V_T) and implantation energy (E_2). Bias conditions are $V_{DS} = 3$V, $I_{DS} = I_{DSS}/2$. (b) Imaginary part of input (Z_1) and output (Z_2) impedance of the same device.

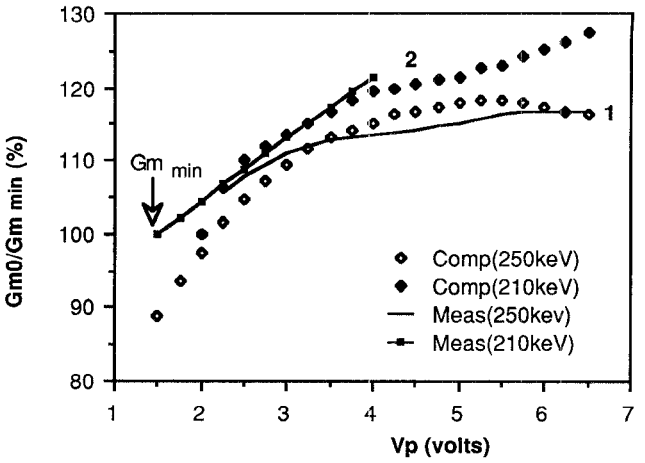


Fig. 11. Computed (scattered points) and measured (solid lines) normalized transconductance ($g_{m0}/g_{m\min}$) versus different pinch-off voltages as obtained by varying the gate recess depth ($g_{m\min} = 90$mS/mm is the smallest transconductance measured). Two wafers realized by double implantation of Si are investigated. Wafer 1, 60 keV–250 keV. Wafer 2, 60 keV–210 keV.

1 V to 2 V) but remain almost constant above $V_T = 2$ V. A similar but opposite tendency is observed for R_{DS}, which initially decreases for $V_T = 1$ V to 2 V and then remains constant (Fig. 5). The rate of R_{DS} increase with recess is relatively faster than the C_{GS} decrease and this explains the greater dependence of output rather than input matching on V_T variations. The large output mismatch created at low V_T's is partly responsible for the smaller amplifier gain.

E. Influence of Profile on Maximum Available Gain (MAG)

Sections III-B to III-D presented the influence of dose, energy, and recess on the amplifier characteristics. The validity of these results was confirmed by investigating the amplifier and FET *MAG* as a function of V_T and E_2. The data obtained in this way depend entirely on profile characteristics since perfect matching is guaranteed at both the input and output. Fig. 10 shows such results for a MESFET at 6.5 GHz. Maximum gain (Fig. 10(a)) is obtained again for $E_2 = 200$ keV (see Section III-C) while no significant *MAG* dependence on V_T is observed. Similar results were obtained for the amplifier by perfect matching of input and output and interstage optimization.

The profile characteristics should not, however, be considered only in terms of their influence on gain. As explained in Section II, III-C and III-D, the E_2, V_T choice also has an effect on the input/output device impedance. For amplifier design this signifies reoptimization of matching in order to benefit from the new gain characteristics. Fig. 10(b) shows the influence of V_T, E_2 on the imaginary part of MESFET input and output impedance (Z_1, Z_2). Z_1 variations are primarily attributed to C_{GS}, while Z_2 changes are due to R_{DS} and g_{m0} [18]. The resistive part of Z_1, Z_2 remains almost constant with V_T, E_2. Process tolerance will also be subjected to the simultaneous effect of gain and matching.

IV. Experimental Results

A. Recess Depth Influence on Device Transconductance

Two series of MESFET's with (1 μm×150 μm) gates have been realized by double Si implantation through 500 Å of Si_3N_4 (series 1: $E_1 = 60$ keV followed by $E_2 = 250$ keV and series 2: $E_1 = 60$ keV followed by $E_2 = 210$ keV). For both series, the dose corresponding to the 60 keV energy was $D_1 = 20\times10^{12}$ cm^{-2}. The dose of the second implantation step was $D_2 = 6\times10^{12}$ cm^{-2}. Different recess depths were realized on the same wafer in order to obtain devices with different pinch-off voltages ranging from 2 V to 6 V. For each device the transconductance g_{m0} was measured. The comparison with the theoretical values is shown in Fig. 11, where the relative transconductance is plotted versus the pinch-off voltage.

When the implantation energy increases (series 1) g_{m0} decreases and its dependence on recess depth becomes smaller. The simulations are in good agreement with these experimental results and indicate that the simulator SIMTEC can account equally well for recess depth and doping profile shape.

It is also interesting to note that for given implantation energy, g_{m0} is found to increase with V_T at a much faster rate for low, rather than high, implantation energies. This suggests the use of low energies for applications where the

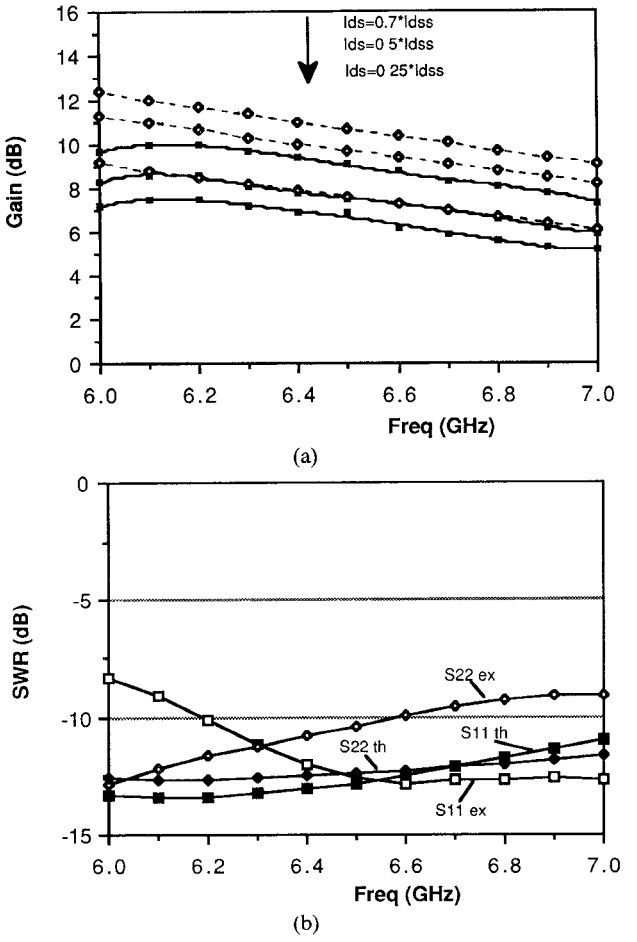


Fig. 12. Experimental (solid lines) and theoretical (dashed lines) microwave performance of the amplifier with $E_2 = 250$ keV, $D_2 = 6\times10^{12}$ cm^{-2} active layers and $V_T = -3.6$ V. The gain (a) is plotted as a function of the drain–source current $I_{DS} = 0.7I_{DSS}$, $0.5I_{DSS}$ and $0.25I_{DSS}$ (I_{DSS} = saturation current). The input and output SWR (b) are plotted for $I_{DS} = 0.5I_{DSS}$.

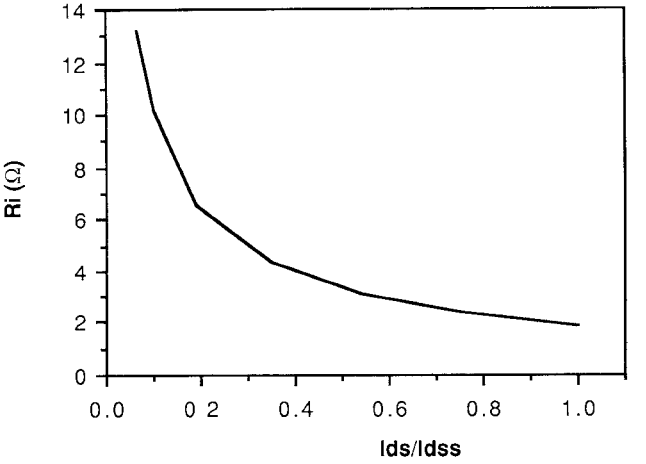


Fig. 13. Computer variations of R_i versus I_{DS}. The FET is the same as in Fig. 2.

g_{m0} improvement is absolutely essential. It also indicates that recessing and, therefore, process variations will have less influence on the transistor g_m if high energy profiles are chosen [7], [9].

B. Bias Influence on Amplifier Performance

The influence of bias on the performance of the two-stage tree amplifier is finally shown in Fig. 12(a) and (b). This study allowed also a first comparison between experimental and theoretical results for the amplifier. The simulations were made using the EESOF Package Touchstone [23] and include consideration of: (i) all "parasitic" connections between MMIC components, bias pads, and ground, (ii) the external biasing capacitances (50 pF) necessary for better RF grounds, and (iii) transitions to the tapered coplanar lines of the test package. The influence of other effects, such as parasitic capacitances of lumped elements and losses of transmission lines and components, have also been considered.[1]

[1]The final circuit file, together with other relevant information, is not given due to limited space, but it will be supplied by the authors upon request.

In Fig. 12(a), the amplifier gain G is plotted over the frequency band of 6 to 7 GHz for bias operating conditions corresponding to $0.7I_{DSS}$, $0.5I_{DSS}$, and $0.25I_{DSS}$. The agreement between theory and experiment is very satisfactory (between 1 and 2.5 dB) in spite of the fact that (i) the experimental results are average values among five chips of the wafer and the relative dispersion of the measurements is $\Delta G = \pm 2.0$ dB; (ii) the g_m values used in the circuit simulations (170 mS/mm at I_{DSS}) were calculated by the presented MESFET model; these are in good agreement with measured values of carefully selected discrete devices (see agreement in Fig. 2), but are, in fact, slightly higher than the measured integrated transistors; and (iii) the measurements are made at the plane of the package connectors since no monolithic calibration standards were available. The precision measurement technique reported earlier [24] could not be applied because the amplifier was designed for use in a package. As shown by both the theoretical and the experimental results, a change in the drain–source current from $0.25I_{DSS}$ to $0.7I_{DSS}$ produces an overall gain improvement. This can be understood by considering the g_m, C_{GS} increase, as well as the R_{DS}, R_i variations: (i) g_m varies with I_{DS} faster than C_{GS}; (ii) R_{DS} decreases with I_{DS} but changes at about the same rate as C_{GS}; (iii) the intrinsic gate resistance R_i reduces by as much as 54 percent when biasing at $0.7I_{DSS}$ instead of $0.25I_{DSS}$ (Fig. 13). In fact, the rate of R_i change with I_{DS} is much faster than for C_{GS} and, combined with the variations of g_m and R_{DS}, results in a larger FET and amplifier gain.

A comparison between theoretical and experimental results concerning the input and output SWR is given in Fig. 12(b), for a biasing $V_{GS} = 3$ V, $I_{DS} = 0.5I_{DSS}$. The agreement is excellent and the differences of input SWR in the range of 6–6.5 GHz can be accounted for by the lack of exact calibration, as discussed earlier.

V. Conclusions

A device simulator called SIMTEC has been presented and applied to ion-implanted MESFET's. Although based on a certain number of assumptions, like most models of

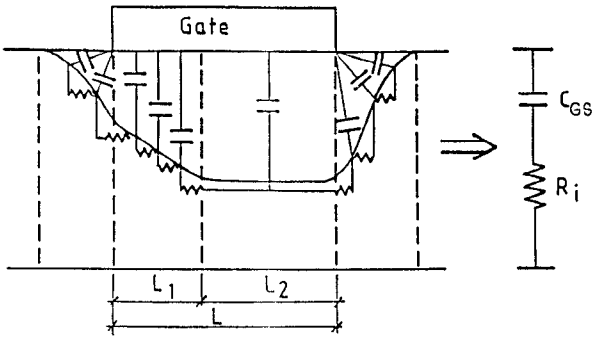


Fig. 14. Transmission line model used for the calculation of the input network $R_i - C_{GS}$. Only eight cells are presented, each corresponding to a cascaded uniform line, but 20 are used in the simulation.

this kind, it proved to be efficient for the technology and process simulation of individual devices and multistage MMIC amplifiers. A good qualitative and quantitative understanding of MESFET and MMIC amplifier influence by implantation dose, energy, recess, and bias conditions was possible. The amplifier gain agreement between theory and experiment is very satisfactory and *SWR* agreement is also very good. SIMTEC is therefore suitable for computer-assisted optimization of MMIC's with respect to processing and sensitivity to technology dispersions.

The results obtained for a two-stage MMIC amplifier show that the gain and input *SWR* are not very sensitive to the implanted dose as long as this exceeds 6×10^{12} cm^{-2}. Implantation energies larger than 200 keV led to smaller gain and *SWR* dispersion. Recess depths should finally be small ($V_T > 2$ V) for the microwave performance to become insensitive to recess variations.

An improvement of MMIC performance and processing yield can therefore be expected by the use of the developed simulator.

Appendix

The input impedance of a common-source MESFET corresponds to that of a nonuniform $R-C$ transmission line (Fig. 14) made of (i) the distributed capacitance of the space charge below the gate (or below the surface of the uncovered active layer) and (ii) of the distributed resistance of the neutral channel. The transmission line is loaded at its drain end by the saturated section of the channel and can therefore be considered as open-circuited.

The computations of the nonuniform line input impedance were performed by cascading about 20 different $R-C$ transmission lines, each of them being considered uniform (Fig. 14). The input impedance of all these cascaded lines can therefore be easily obtained and the real part of it is equal to the intrinsic channel resistance R_i.

C_{GS} can be obtained either from the imaginary part of the impedance or from the incremental charge of the stored charge below the gate corresponding to a variation of intrinsic gate voltage. Both techniques yield similar results.

Finally, the edge effects are implicitly included in the present calculations since the space charge below the surface (due to Fermi level pinning) and at the gate edges is considered.

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The simulations reported in this work were performed at the computer facilities at the University of Michigan, and the continuous help and support of the computing staff, in particular C. Nicholas, are greatly acknowledged.

References

[1] J. Higgins, "Modeling the influence of carrier profiles on MESFET characteristics," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1066–1073, June 1980.

[2] R. Trew, A. Khatibzadeh and N. Masnari, "Deep-level and profile effects upon low-noise ion-implanted GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 877–882, May 1985.

[3] J. Golio and R. Trew, "Profile studies of ion-implanted MESFET's," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1866–1869, Dec. 1983.

[4] M. Shur and L. Eastman, "$I-V$ characteristics of GaAs MESFET with nonuniform doping profile," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 455–461, Feb. 1980.

[5] P. DeSantis, "Extension of existing model to ion-implanted MESFET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 638–647, June 1980.

[6] T. Chen and M. Shur, "Analytical models of ion-implanted GaAs FET's," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 18–28, Jan. 1985.

[7] J. L. Cazaux, J. Graffeuil, and M. Pouysegur, "Profile effects upon electrical performance and linearity of GaAs MESFETs," submitted to *Proc. Inst. Elec. Eng.*

[8] R. A. Pucel, H. Statz, and H. A. Haus, "Signal and noise properties of gallium arsenide microwave field effect transistors," in *Advances in Electronics and Electron Physics*, vol. 38. New York; Academic Press, 1975, pp. 195–265.

[9] J. L. Cazaux, J. Graffeuil, and D. Pavlidis, "Optimisation du Profil de Dopage d'un MESFET Realise par Implantation Ionique," *Rev. Phys. Appl.*, vol. 21, pp. 139–149, Feb. 1986.

[10] J. Graffeuil and P. Rossel, "Semi-empirical expression for direct transconductance and equivalent saturated velocity in short-gate-length MESFET's, *Proc. IEEE*, vol. 129, part I, pp. 185–188, Oct. 1982.

[11] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[12] C. Kokot and A. Stolte, "Backgating effects in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1059–1064, July 1982.

[13] N. Song, D. P. Meikirk, and T. Itoh, "Modeling of ion-implanted GaAs MESFET's by finite element method," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 208–210, Apr. 1986.

[14] A. B. Grebene and S. K. Ghandi, "General theory for pinched operation of the junction gate FET," *Solid State Electron.*, vol. 12, 1969.

[15] W. Dingfen and K. Heime, "New explanation of N_D^{-1} dependence of specific contact resistance for N-GaAs," *Electron. Lett.*, vol. 18, no. 22, pp. 940–941, Oct. 1982.

[16] R. Gorg and I. J. Bohl, "Characteristics of Coupled Microstrip Lines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, p. 700, July 1979.

[17] Y. Ayasli, "Microwave switching with GaAs FET's," *Microwave J.*, pp. 61–74, Nov. 1982.

[18] R. Soares, J. Graffeuil, and J. Obregon, *Applications of GaAs MESFETs*. New York: Artech House, 1983, pp. 13–78; also "Applications des Transistors a Effet de Champ en Arseniure de Gallium," (Editor, Eyrolles, Paris, 1984).

[19] W. Wisseman and M. Macksey, "GaAs microwave devices and circuits with submicron electron beam defined features," *Proc. IEEE*, vol. 71, p. 667, May 1983.
[20] D. Pavlidis and J. Magarshack, "A two-stage modular cell monolithic amplifier," presented at 8th European Specialist Workshop on Active Microwave Semiconductor Devices London, May 1983.
[21] D. Pavlidis, Y. Archambault, M. Efthimerou, D. Kaminsky, A. Bert and J. Magarshack, "A new specifically monolithic approach to microwave power amplifiers," in *Proc. 1983 IEEE Microwave Millimeter-Wave Monolithic Symp.* (Boston), May–June 1983, pp. 54–58.
[22] M. Weiss and D. Pavlidis, "Power optimization of GaAs implanted FET's based on large-signal modeling," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 175–188, Feb. 1987.
[23] EESOF - Touchstone Software.
[24] M. Parisot, Y. Archambault, D. Pavlidis and J. Magarshack, "Highly accurate design of spiral inductors for MMIC's with small size and high cutoff frequency characteristics," in *Proc. 1984 Microwave Millimeter-Wave Monolithic Circuits Symp.* (San Francisco), pp. 91–95.

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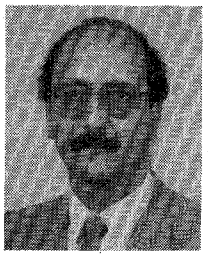

Dimitris Pavlidis (S'73–M'76–SM'83) received the B.Sc. degree in physics from the University of Patras, Greece, in 1972 and the Ph.D. degree in applied science-electronic engineering from the University of Newcastle-upon-Tyne, England, in 1976.

From 1975 to 1978, he worked as a Research and Postdoctoral Fellow in the Department of Electrical and Electronic Engineering of Newcastle University. During these years he worked on microwave semiconductor devices and circuits, in particular, the properties of Gunn-effect oscillators employed for fast angle modulation applications. He was also responsible for a program on microwave signal handling for industrial underwater diving projects. In 1978, he joined the High Frequency Institute of Technical University of Dermstadt, West Germany, where he was responsible for establishing a new semiconductor technology facility for GaAs microwave transistors and circuits. As a Lecturer, he was also involved in teaching courses on microwave semiconductor devices and circuits. In 1980, he worked for UNESCO as a consultant at the Central Electronic Engineering Research Institute, Pilani, India.

During the years 1980–1985, Dr. Pavlidis was Engineer and Manager of the GaAs Monolithic Microwave Integrated Circuits (MMIC) Group of Thomson-CSF DHM/DAG, Corbeville, France. In this capacity, he participated in the creation of the new GaAs-IC Division of Thomson-CSF and was involved with technology, process evaluation, design, and testing of MMIC's. He was responsible for a number of research projects on monolithic power and broad-band amplifiers, tunable oscillators, and preamplifiers for optical applications. His work at Thomson was also concerned with the development of monolithic phase shifters, attenuators, and IF amplifiers and the establishment of a component library for MMIC applications. In 1986 Dr. Pavlidis was appointed Professor of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor. His current research interests cover the design and fabrication of HEMT's, HBT's, strained heterostructures, and III–V microwave and millimeter devices and IC's.

Dr. Pavlidis's publications are in the area of microwave semiconductor devices and circuits. He holds six patents on MMIC applications and has written several Thomson reports in this area. He was Chairman of the 7th European Specialist Workshop on Active Microwave Semiconductor Devices (AMSD), Spetsai, Greece, 1981, and Secretary of the 11th International Symposium on GaAs and Related Compounds, Biarritz, France, 1984.

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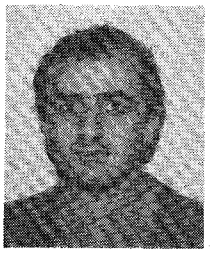

Jean-Louis Cazaux was born in 1960 in Tarbes, France. He received his first degree in physics from the Université Paul Sabatier, Toulouse, France, in 1982 and the Ph.D in electronics from the Institut National des Sciences Appliquées, Toulouse, in 1985.

From 1982 to 1986 he worked at the L.A.A.S. laboratory of the Centre National de le Recherche Scientifique, Toulouse, on the modeling and applications of GaAs MESFET's with non-uniform doping profile. In 1987, he was a post-doctoral research fellow with the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor. His research concerned the design of HEMTs and other III–V microwave devices as applied in monolithic microwave integrated circuits (MMIC). In 1988, he joined Alcatel-Espace, Toulouse, as design engineer of MMIC's for spatial applications.

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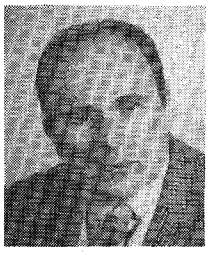

Jacques Graffeuil was born in Agen, France. He received the Ingenieur I.N.S.A. degree and the These d'Etat in electronic engineering in 1969 and 1977, respectively, both from Paul Sabatier University, Toulouse, France.

Since 1970, he has been an Assistant Professor at Paul Sabatier University. At the same time, he joined the Laboratoire d'Automatique et d'Analyse des Systèmes du Centre National de la Recherche Scientifique, Toulouse, where he was engaged in research on noise in semiconductor devices. His first area of interest was Gunn effect devices. Since 1972 he has been involved with the study of gallium arsenide Schottky-barrier FET's. He is currently Professor of Electrical Engineering at Paul Sabatier University, Toulouse, France. His current activities are in the area of MESFET's and GaAlAs/GaAs FET's.

Dr. Graffeuil has authored or coauthored over 30 technical papers and three books.